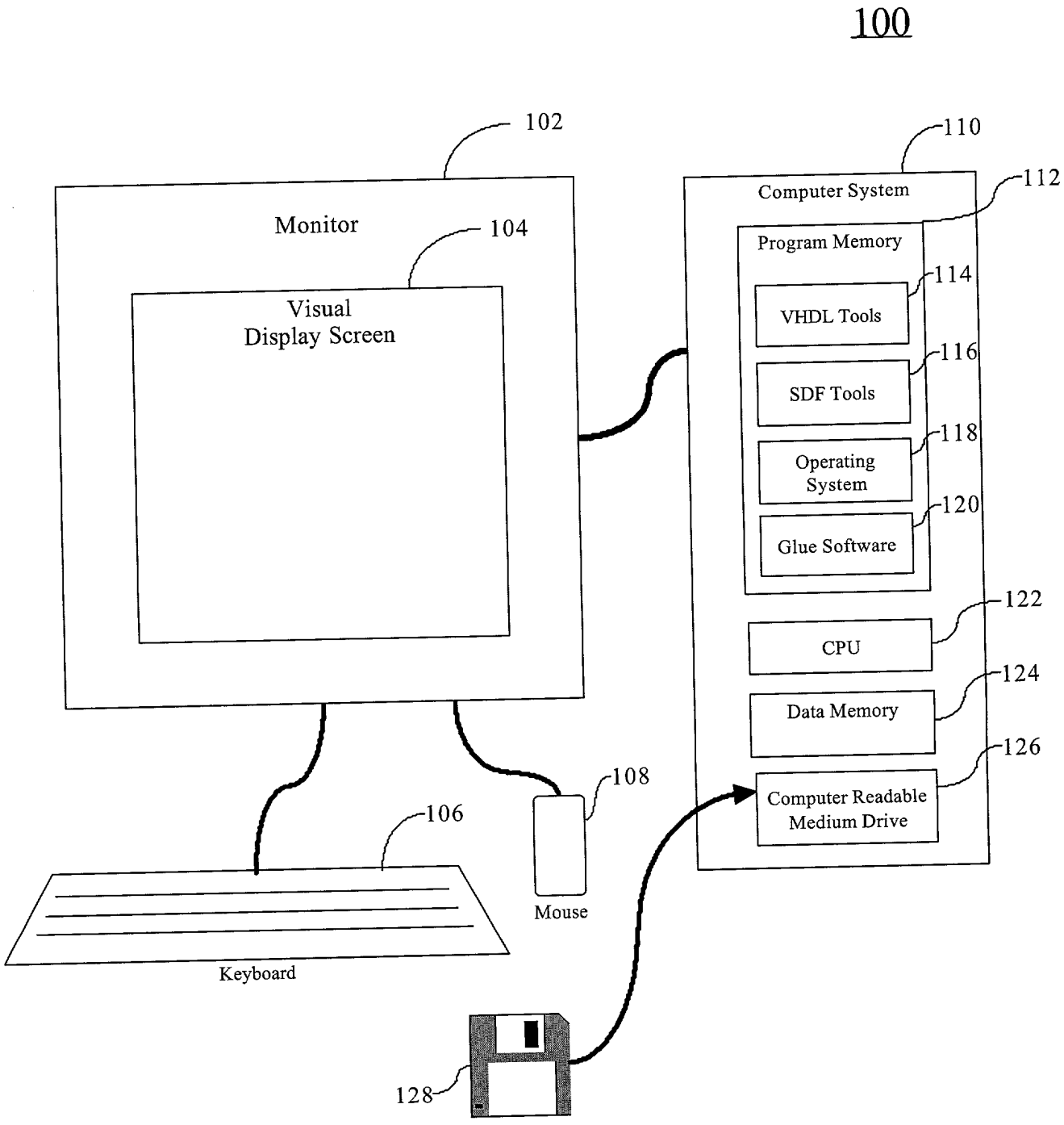

100
102
Monitor
104
Visual
Display Screen
110
Computer System
112
Program Memory
114
VHDL Tools
116
SDF Tools
118
Operating
System
120
Glue Software
122
CPU
124
Data Memory
126
Computer Readable
Medium Drive
108
Mouse
106
Keyboard
128

FIG 1

112

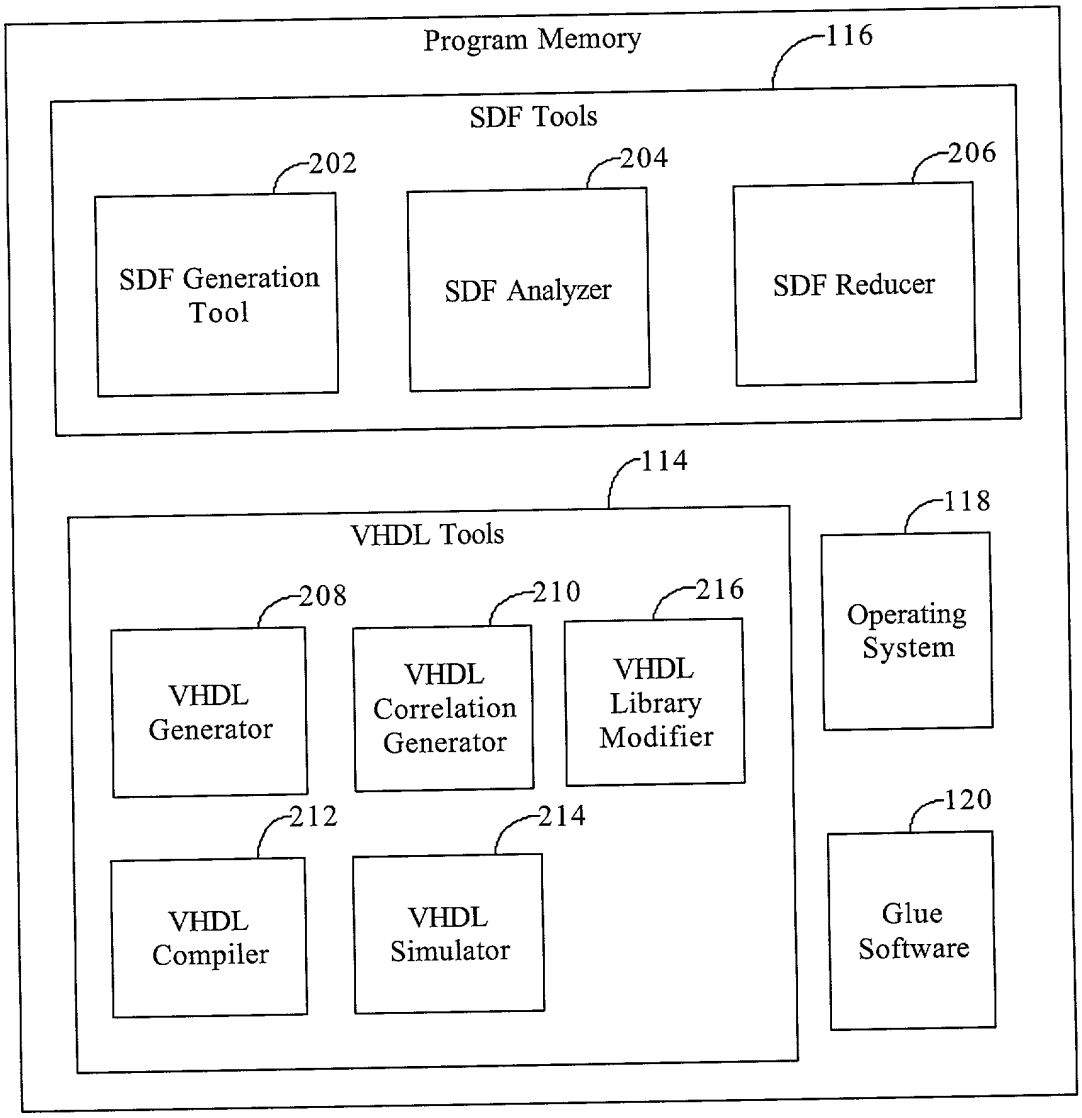

Program Memory
116
SDF Tools
202
SDF Generation Tool
204
SDF Analyzer
206
SDF Reducer
114
VHDL Tools
208
VHDL Generator
210
VHDL Correlation Generator
216
VHDL Library Modifier
212
VHDL Compiler
214
VHDL Simulator
118
Operating System
120
Glue Software

FIG 2

124

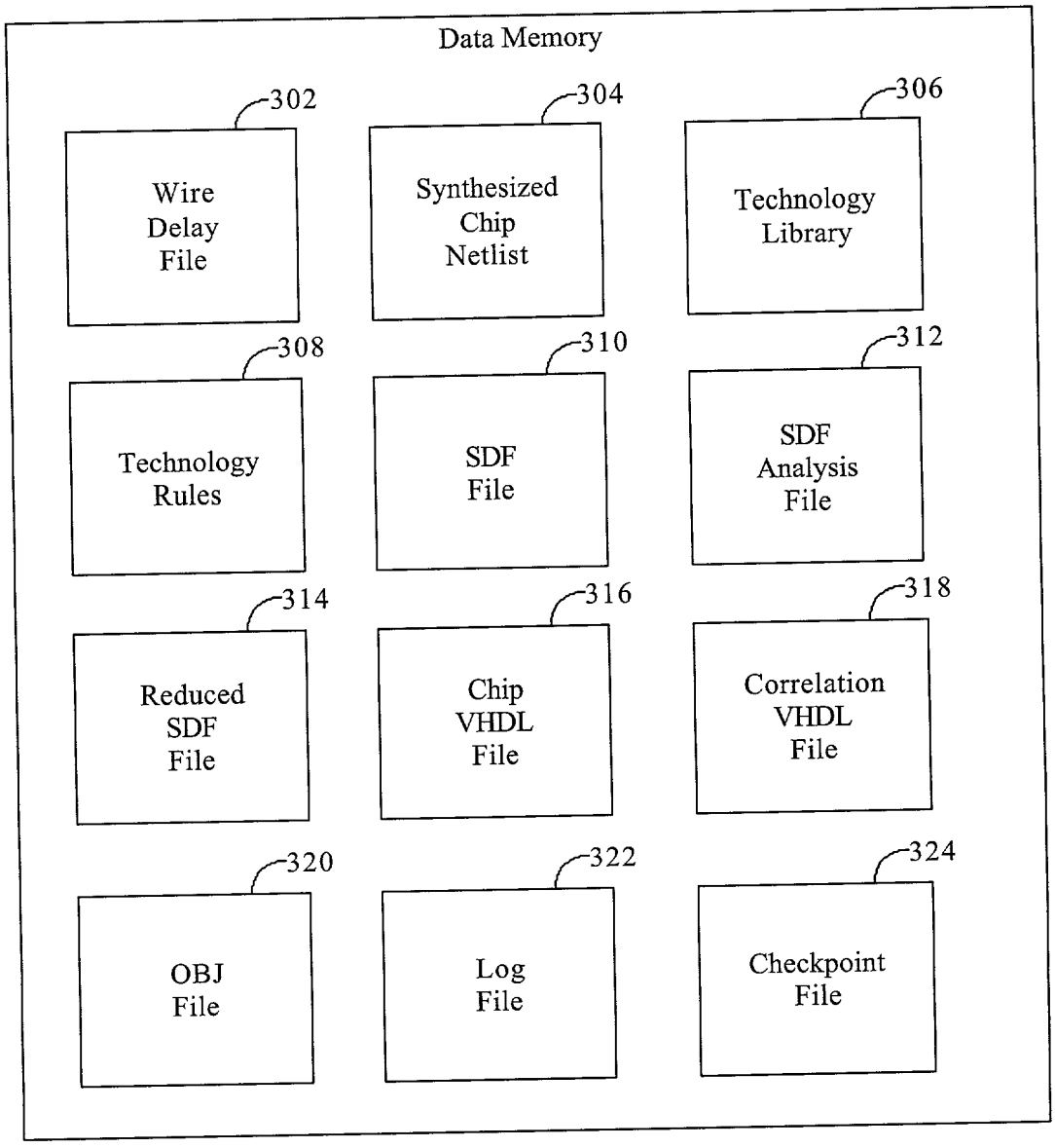

Data Memory
302
Wire Delay File
304
Synthesized Chip Netlist
306
Technology Library
308
Technology Rules
310
SDF File
312
SDF Analysis File
314
Reduced SDF File
316
Chip VHDL File
318
Correlation VHDL File
320
OBJ File
322
Log File
324
Checkpoint File

FIG 3

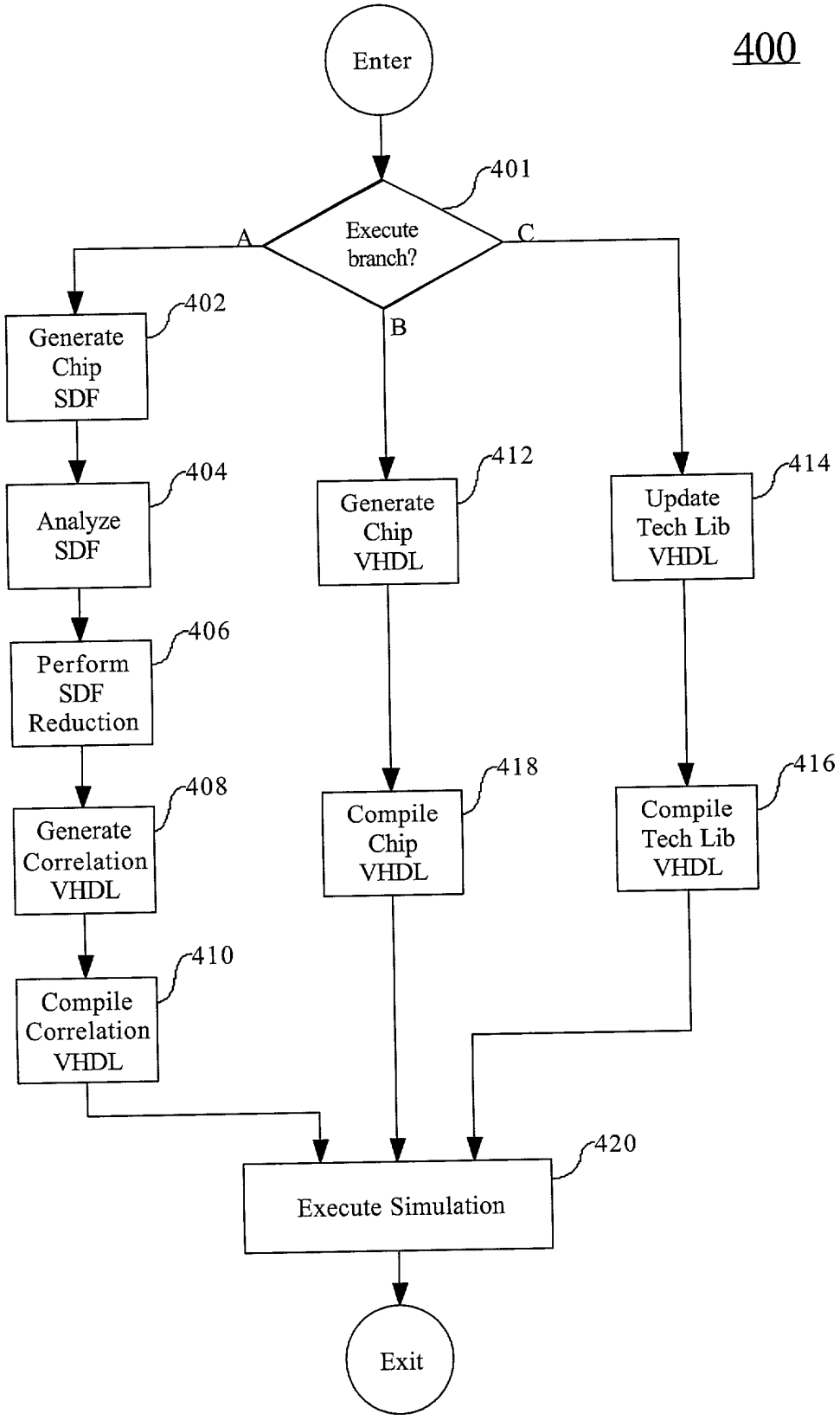

400
Enter
401
Execute branch?
A
B
C
402
Generate Chip SDF
404
Analyze SDF
406
Perform SDF Reduction
408
Generate Correlation VHDL
410
Compile Correlation VHDL
412
Generate Chip VHDL
418
Compile Chip VHDL
414
Update Tech Lib VHDL
416
Compile Tech Lib VHDL
420
Execute Simulation
Exit

FIG 4

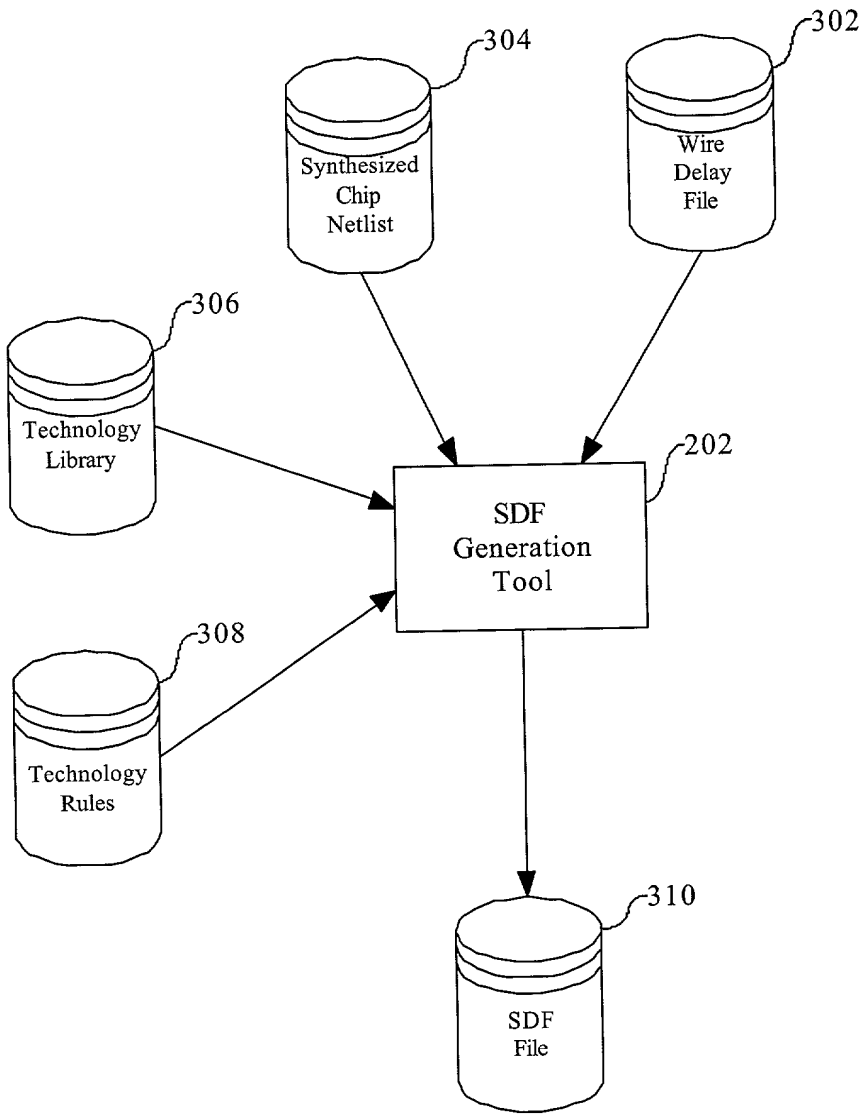

402
304
302
Synthesized Chip Netlist
Wire Delay File
306
Technology Library
202
SDF Generation Tool
308
Technology Rules
310
SDF File

FIG 5

404

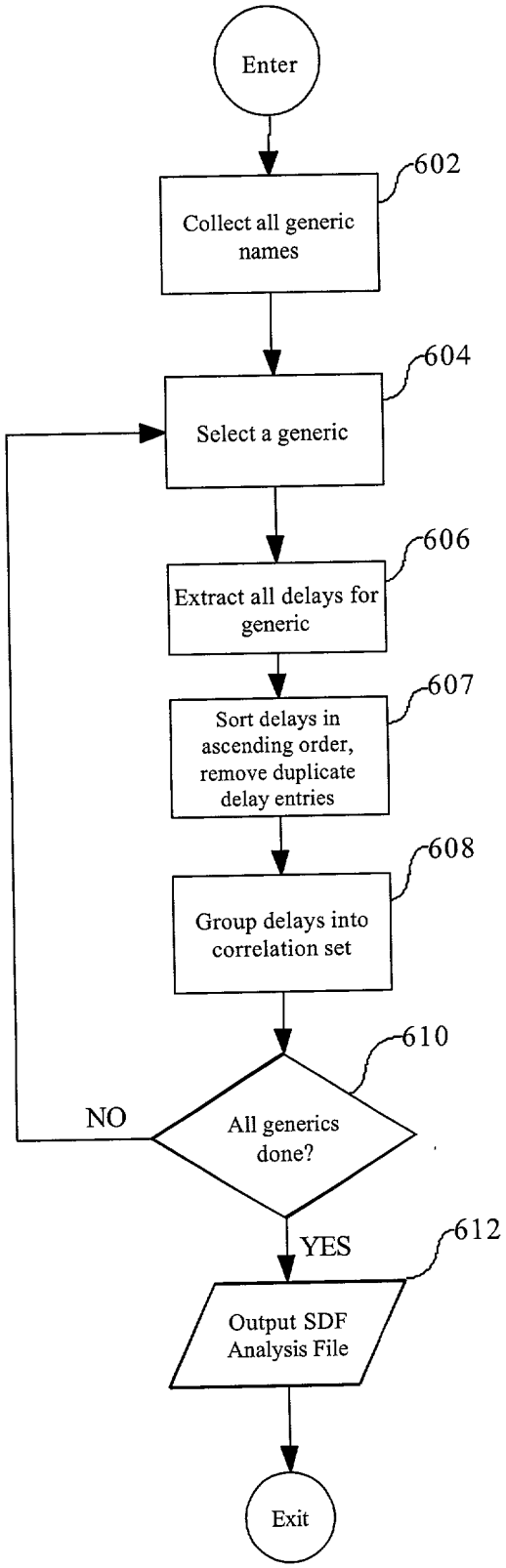

Enter
602
Collect all generic names
604
Select a generic
606
Extract all delays for generic
607
Sort delays in ascending order, remove duplicate delay entries
608
Group delays into correlation set
610
All generics done?
NO
YES
612
Output SDF Analysis File
Exit

FIG 6

700

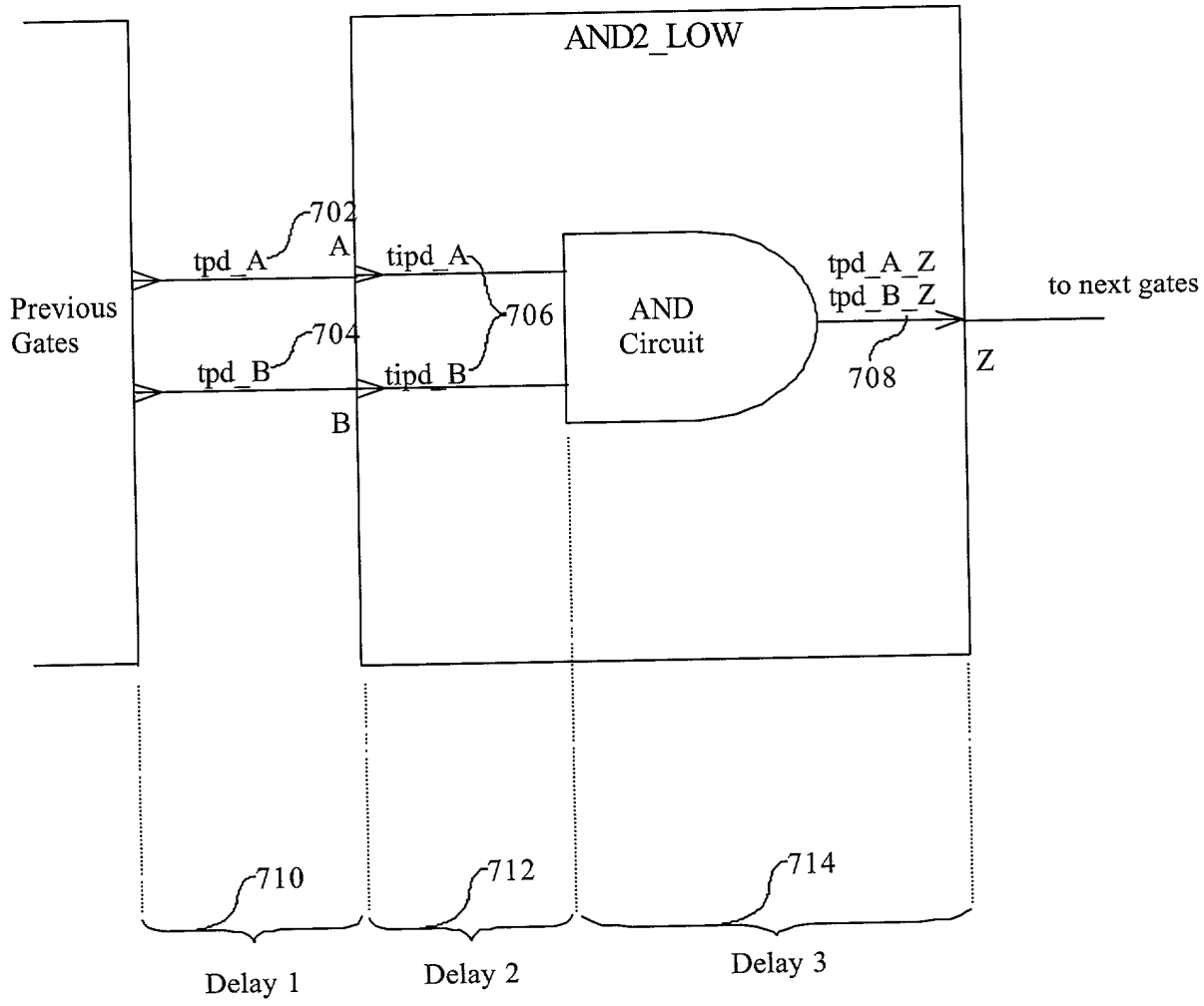

AND2_LOW
Previous Gates
tpd_A
702
A
tipd_A
tpd_B
704
tipd_B
B
706
AND Circuit
tpd_A_Z
tpd_B_Z
708
Z
to next gates
710
712
714
Delay 1
Delay 2
Delay 3

FIG 7

800

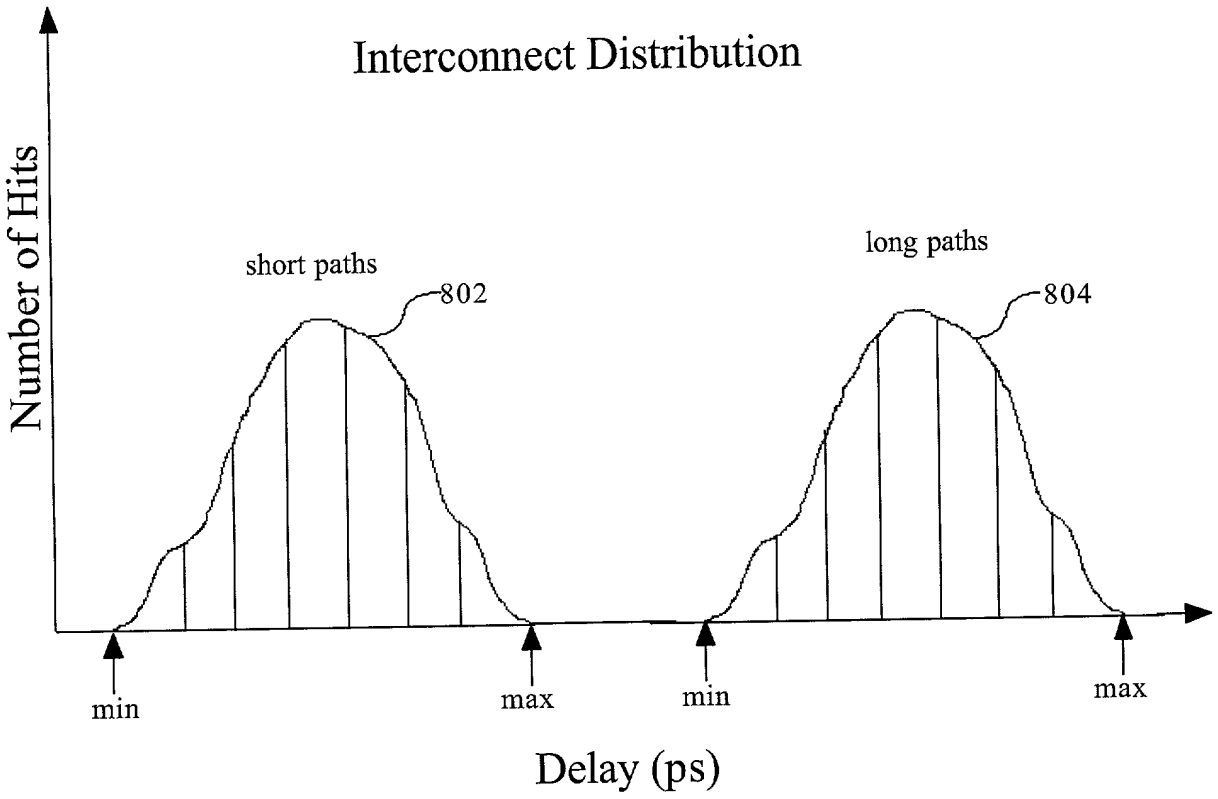

Interconnect Distribution
Number of Hits
short paths
802
long paths
804
min
max
min
max
Delay (ps)

FIG 8

900

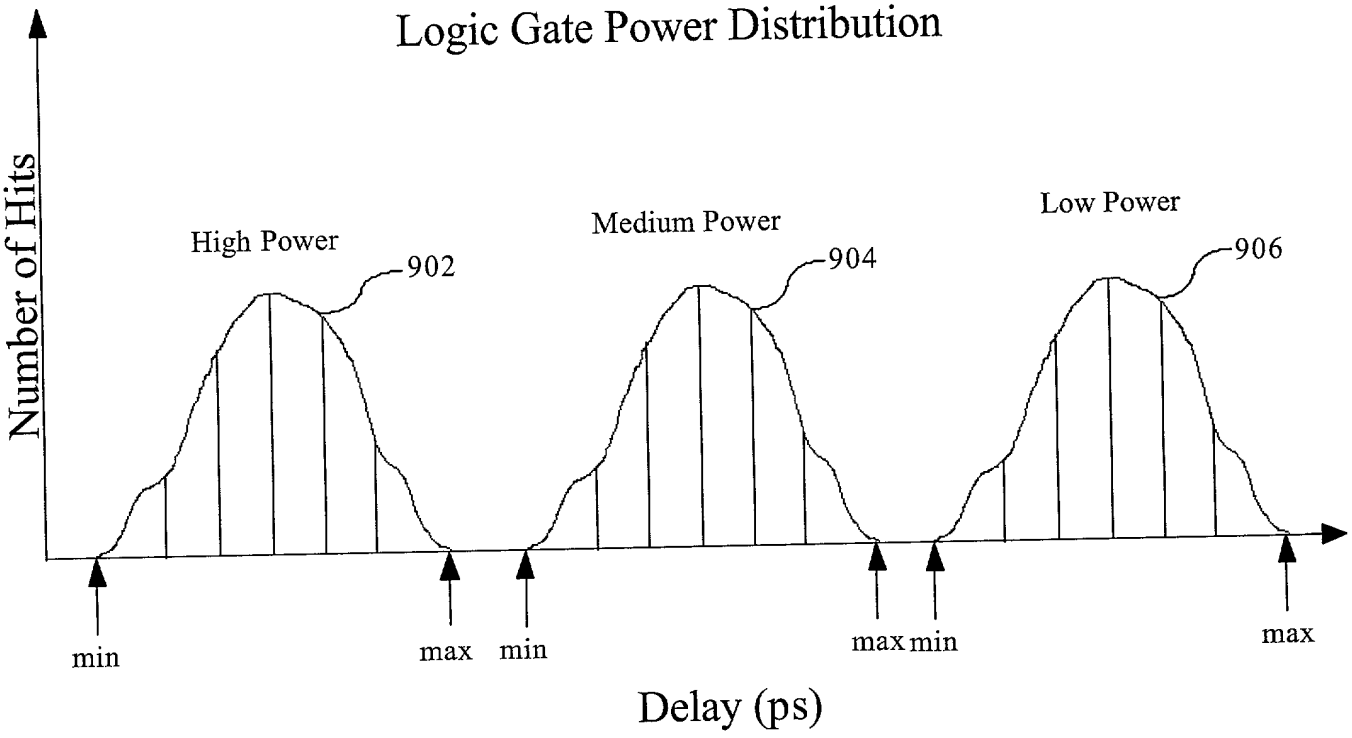

Logic Gate Power Distribution
Number of Hits
High Power
902
Medium Power
904
Low Power
906
min
max
min
max
min
max
Delay (ps)

FIG 9

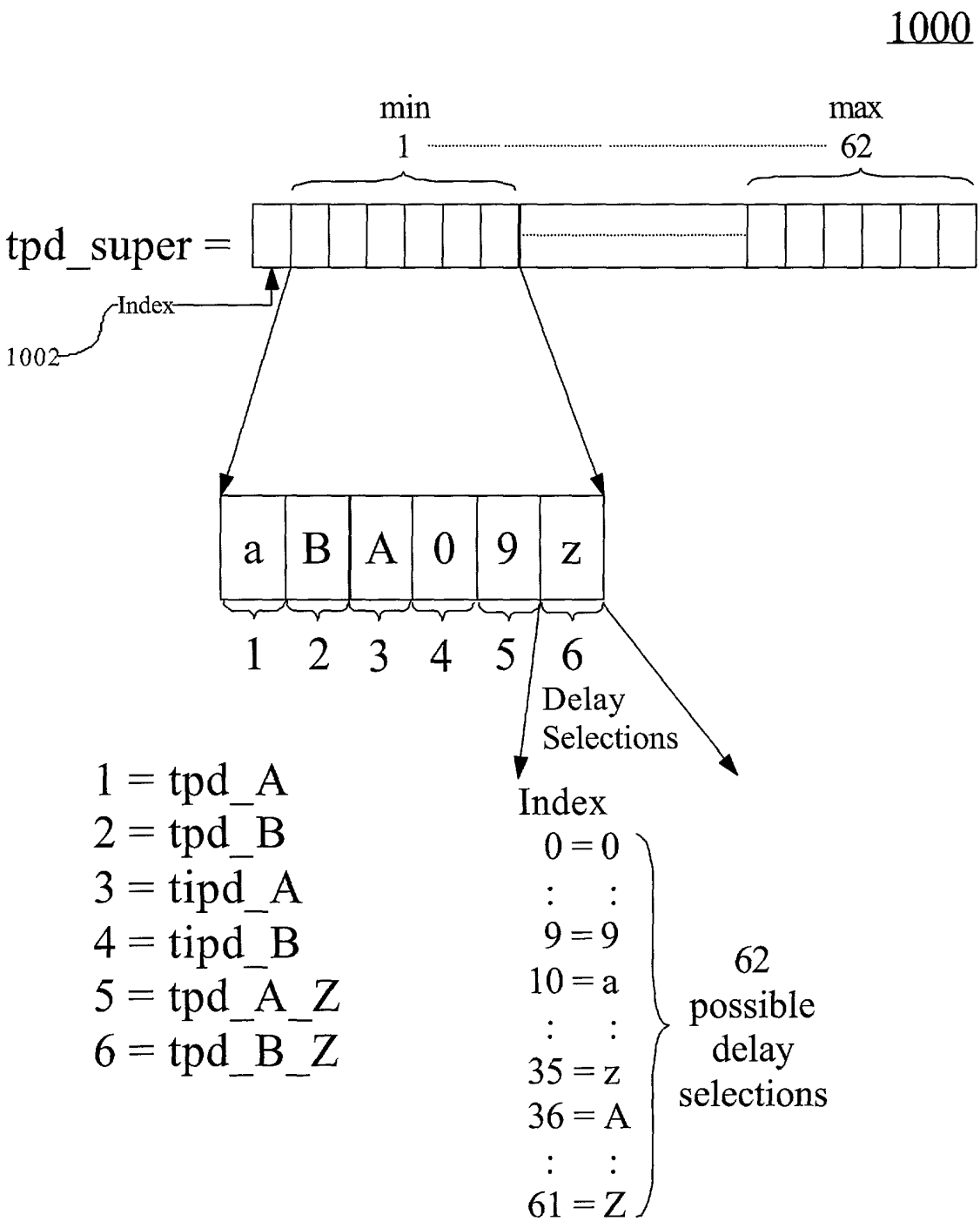

1000
min
1
max
62
tpd_super =
Index
1002
a
B
A
0
9
z
1
2
3
4
5
6
Delay
Selections
1 = tpd_A
2 = tpd_B
3 = tipd_A
4 = tipd_B
5 = tpd_A_Z
6 = tpd_B_Z
Index
0 = 0
9 = 9
10 = a
35 = z
36 = A
61 = Z
62
possible
delay
selections

FIG 10

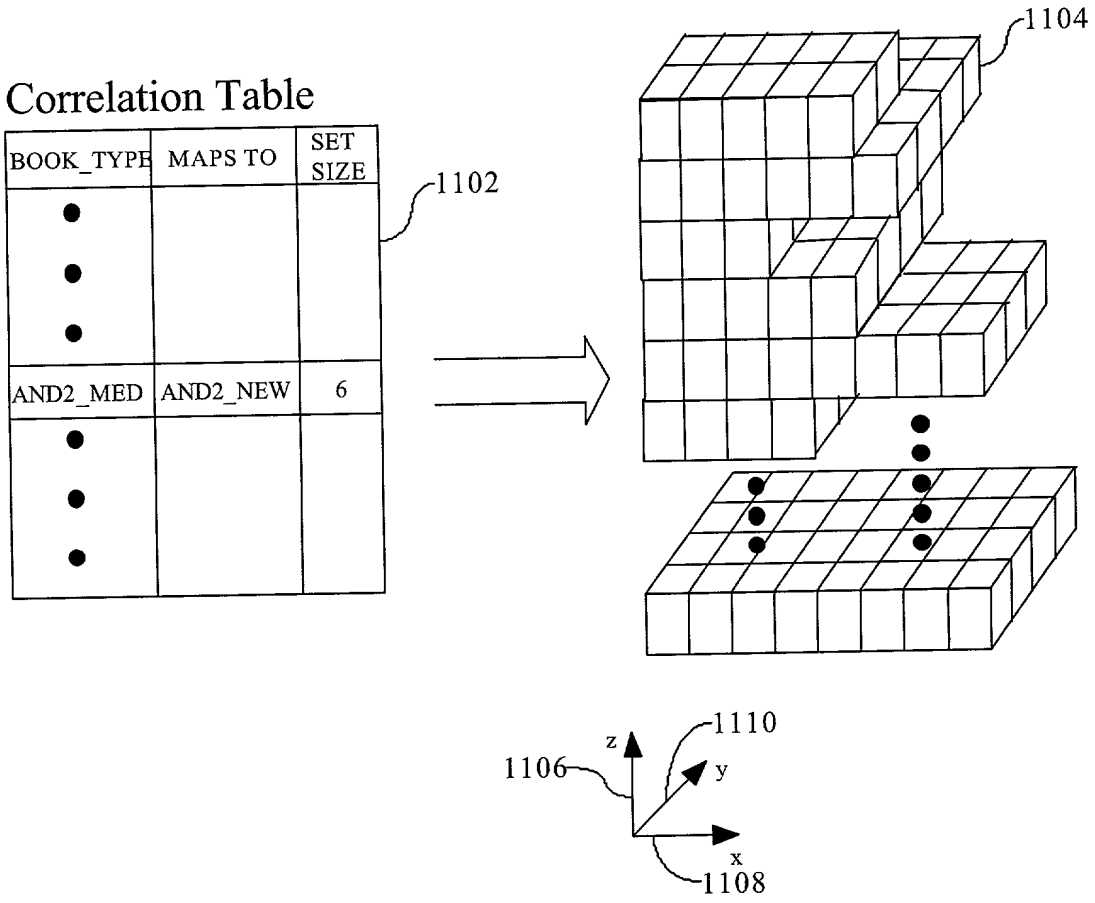

1100
Correlation Table
BOOK_TYPE
MAPS TO
SET SIZE
AND2_MED
AND2_NEW
6
1102
1104
1106
1108
1110
z
y
x

FIG 11

1200

CHAR POSITION (0 OFFSET)	CHAR VALUE	Correlation Set (x')	Entry Position (y')	Slot Offset (x")
0	1	N/A	N/A	N/A
1	4	1	5th	1st
2	X	1	60th	2nd
3	a	1	11th	3rd
4	m	1	26th	4th
5	p	1	29th	5th
6	l	1	25th	6th

FIG 12

1300

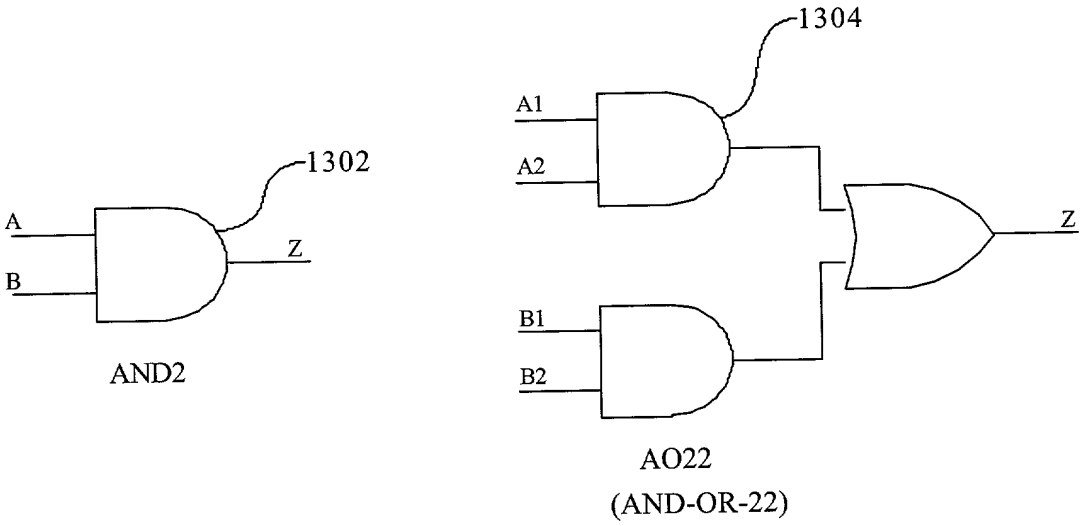


FIG 13

1400

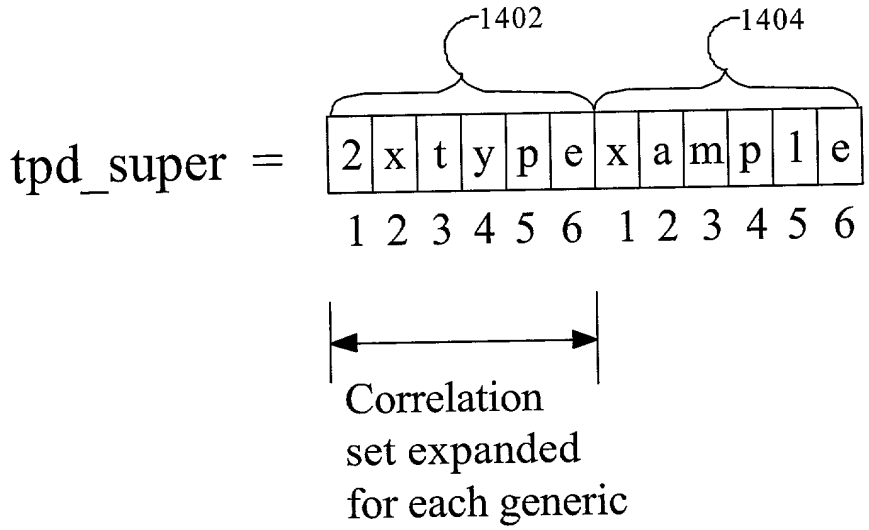

1402
1404
tpd_super =
2 x t y p e x a m p l e
1 2 3 4 5 6 1 2 3 4 5 6
Correlation
set expanded
for each generic
1 → tpd_A
2 → tpd_B
3 → tipd_A
4 → tipd_B
5 → tpd_A_Z
6 → tpd_B_Z

FIG 14

1500

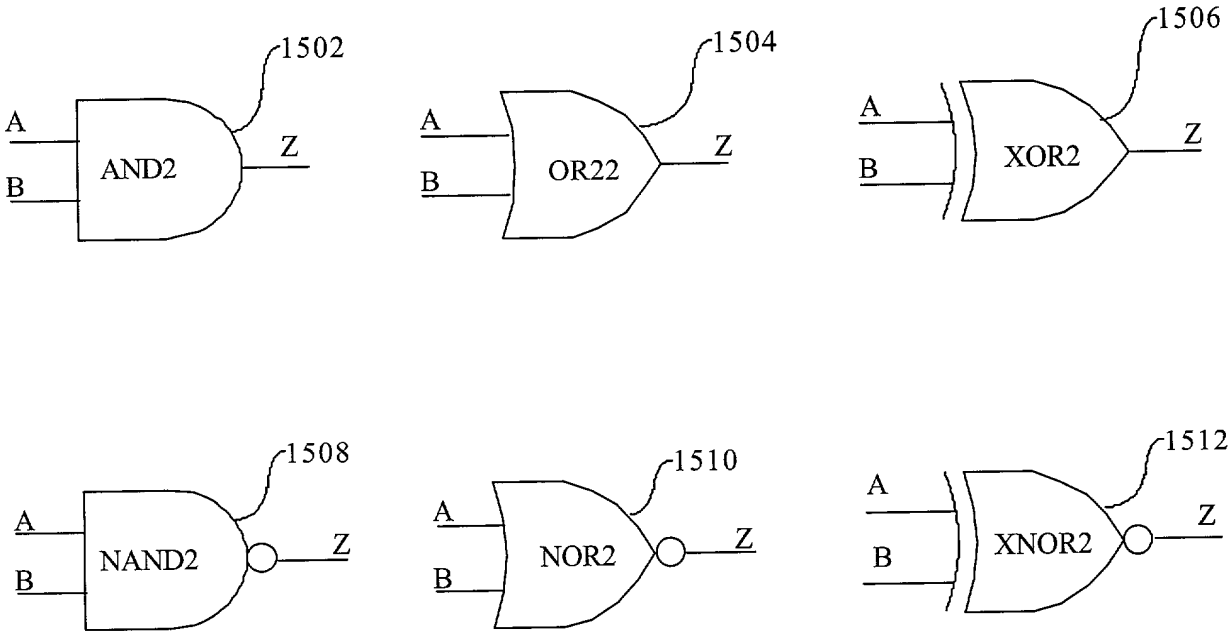
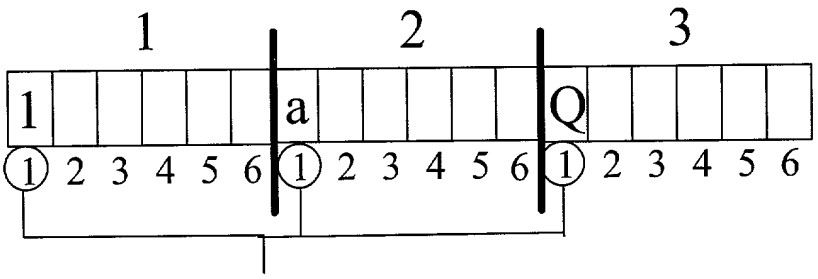

1502
A
B
AND2
Z
1504
A
B
OR22
Z
1506
A
B
XOR2
Z
1508
A
B
NAND2
Z
1510
A
B
NOR2
Z
1512
A
B
XNOR2
Z

FIG 15

1600



tpd_A positions for AND2 gate

Encode as:

DELAY tpd_A

DELAY	1	2	3
-0.500 ns	0	0	0
-0.499 ns	0	0	1
⋮	⋮	⋮	⋮
+237.826 ns	Z	Z	Y
+237.827 ns	Z	Z	Z

FIG 16

1700

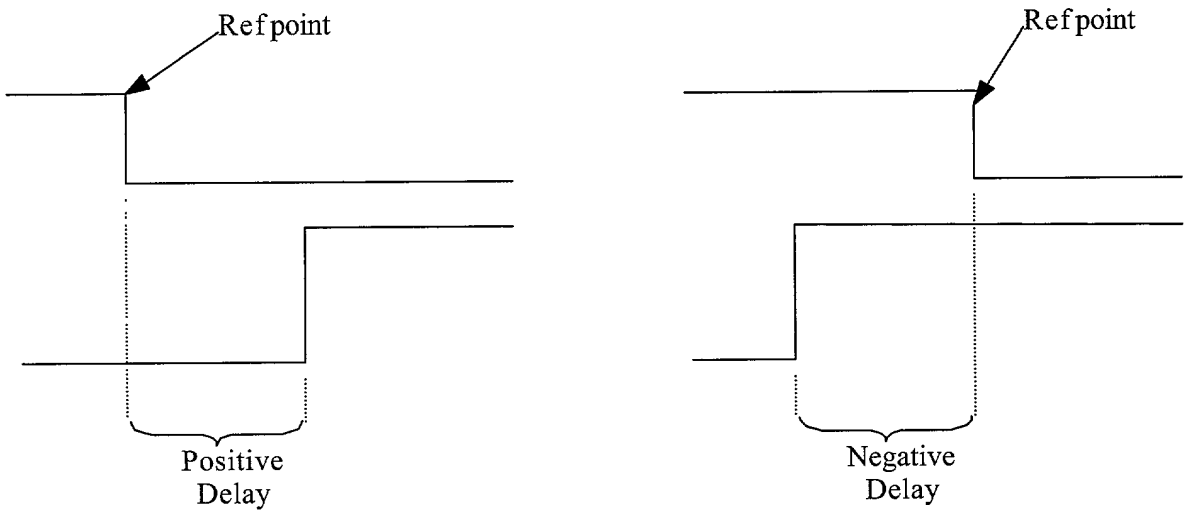


FIG 17

406

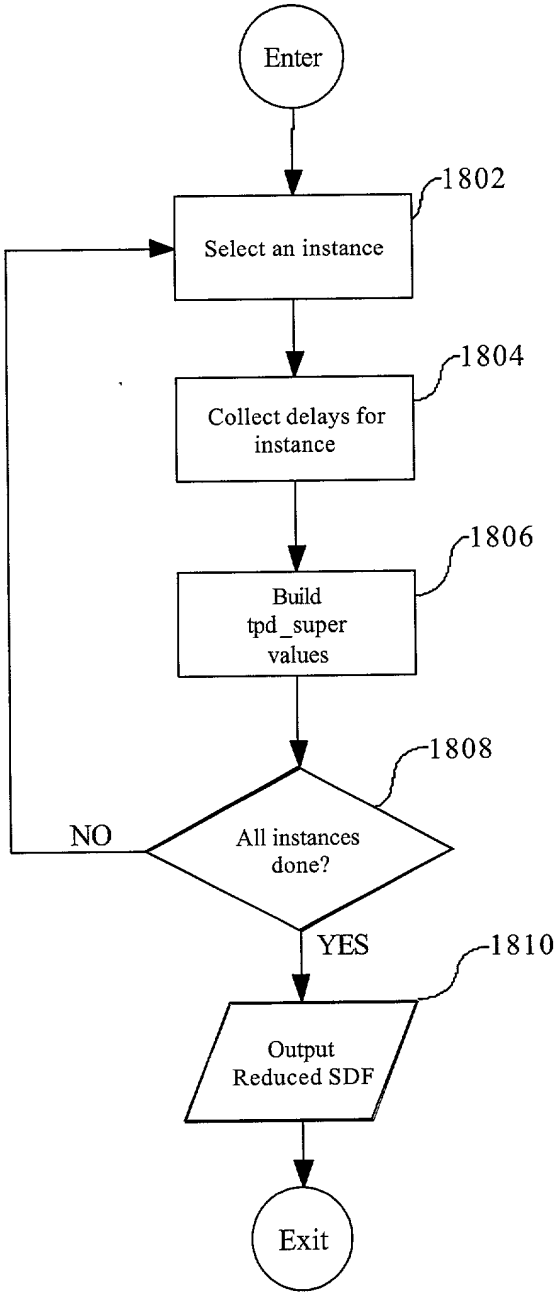

Enter
1802
Select an instance
1804
Collect delays for instance
1806
Build tpd_super values
1808
All instances done?
NO
YES
1810
Output Reduced SDF
Exit

FIG 18

408

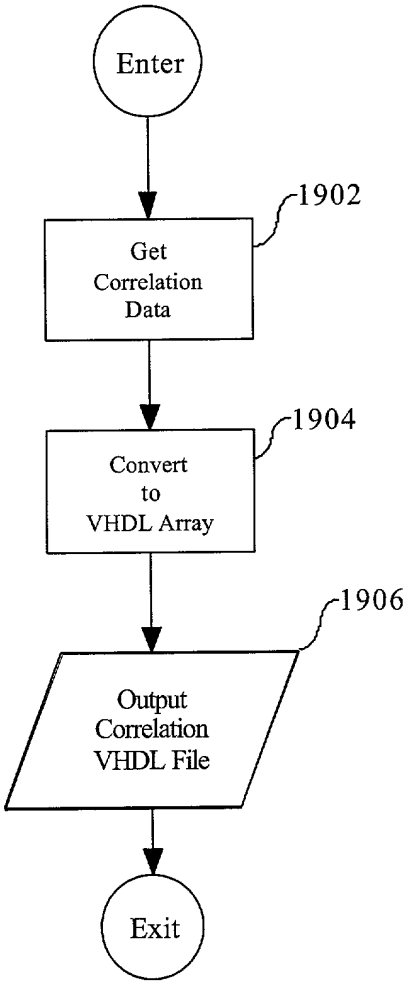

Enter
1902
Get
Correlation
Data
1904
Convert
to
VHDL Array
1906
Output
Correlation
VHDL File
Exit

FIG 19

412

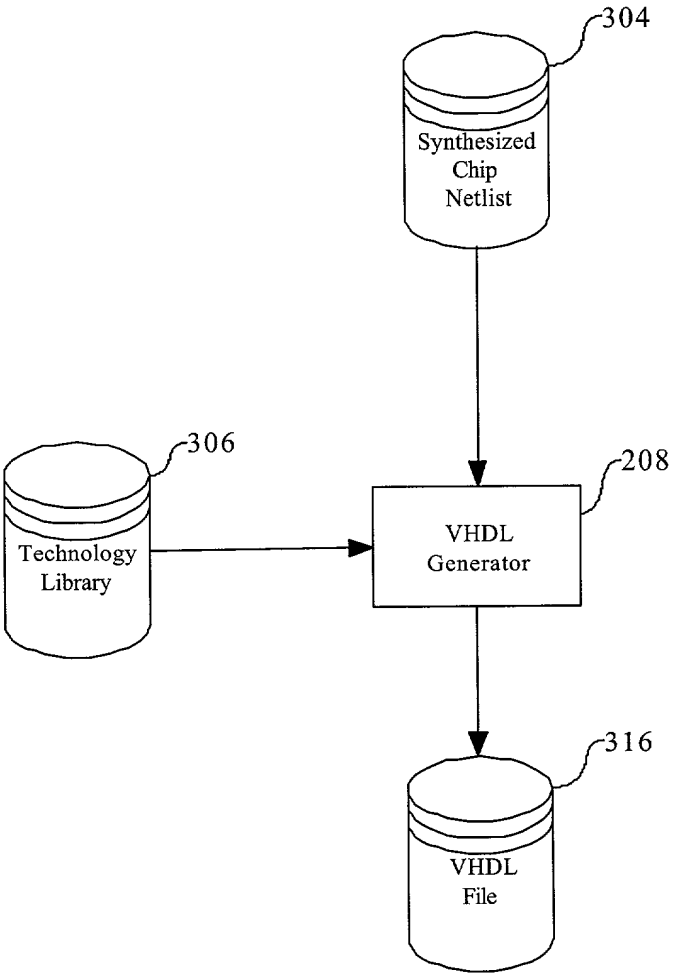

304
Synthesized Chip Netlist
306
Technology Library
208
VHDL Generator
316
VHDL File

FIG 20

418

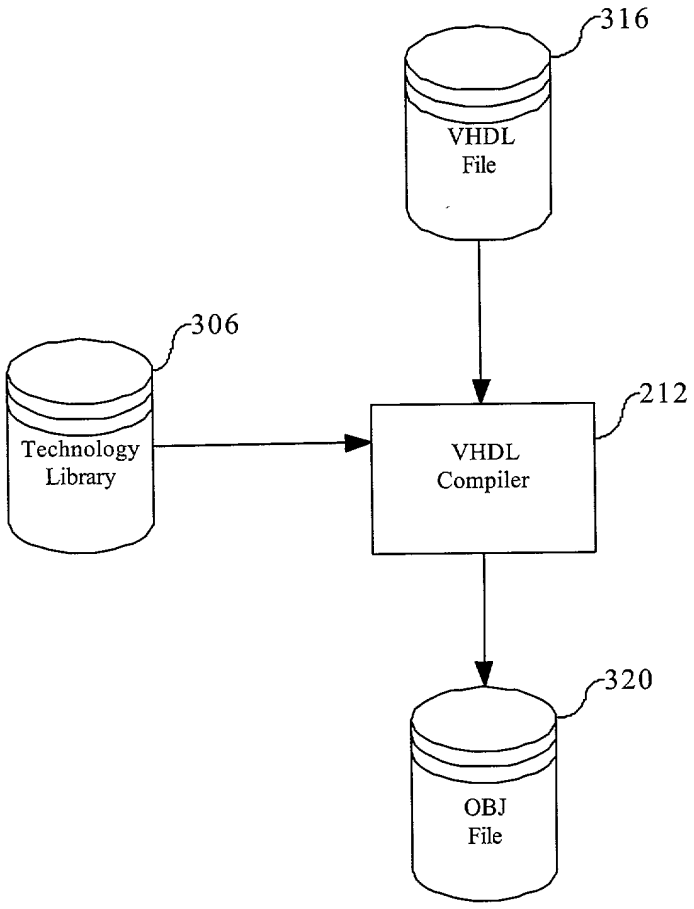

316
VHDL
File
306
Technology
Library
212
VHDL
Compiler
320
OBJ
File

FIG 21

420

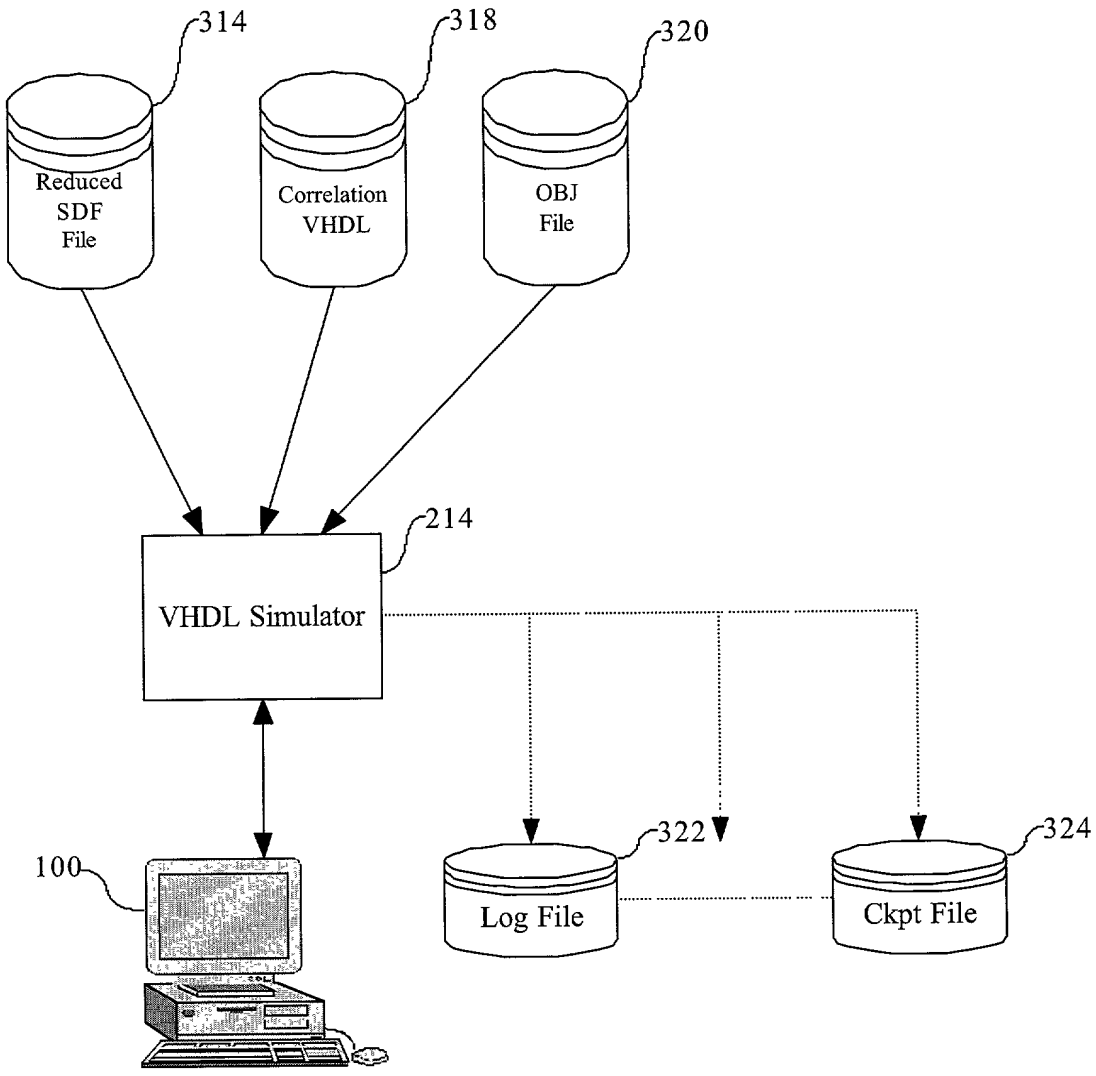

314
318
320
Reduced SDF File
Correlation VHDL
OBJ File
214
VHDL Simulator
100
322
324
Log File
Ckpt File

FIG 22